Solar Powered Z-Source Neutral Point Clamped Five Level Inverter Performance Analysis by Using SPWM and SVPWM technique

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Abstract – The Scope of this paper is to reduce the harmonic content and to boost the output voltage by introducing an emerging technique termed as Z-Source multilevel inverter. The Z-Source inverter had overcome many drawbacks in traditional inverters (Voltage source & Current source Inverters).The main advantage of Z- Source inverter is the presence of shoot through period (Short circuit) which plays a important role in boosting the voltage .When the number of level in the output voltage of multilevel inverter is increased then accordingly the harmonics content is also reduced. Normally for a multilevel inverter the output voltage is restricted to summation of all the input voltage values .To enhance this feature Z-Source is introduced with multilevel inverter to obtain boosted voltage along with low harmonic distortion .The proposed methodology analysis the Z-Source Neutral point clamped inverter using Space vector modulation technique with MATLAB Simulink model and the related parameters are analyzed.

Index Terms – Boosted output voltage, Neutral Point Clamped Inverter (NPCI), Reduction in harmonic content, Shoot through state, Space Vector Pulse Width Modulation Technique (SVPWM), Z-Source Inverter.

1. INTRODUCTION

In recent years, multilevel inverters have drawn significant attention in research and high power applications such as Flexible AC Transmission Systems (FACTS), renewable energy resources, power quality devices , etc [1]-[4]. Such power converters have been the prime focus of power electronic researches in order to improve their performance, reliable, energy efficient at minimum cost. The important task of multilevel inverter is producing a sinusoidal voltage waveform from DC sources.
The major advantages of multilevel inverters are:

1. High voltage capability with voltage limited devices
2. Low harmonic distortion
3. Reduced switching losses
4. *Increased efficiency*
5. *Good electromagnetic compatibility*

Among several reported topologies, diode-clamped multilevel inverter, cascaded H-bridge multilevel inverter and flying capacitor multilevel inverter are very used [2]. To control these multilevel inverters several carrier-based PWM strategies and space vector PWM (SVPWM) have been reported [11]-[12]. Some other methods such as harmonic optimization attempt to reduce or eliminate harmonic in multilevel inverters [3].

Traditional inverters are known to produce an output voltage that is lower than the DC source voltage. In order to reach boosted voltage with available switching devices Z-Source inverters were invented in 2003 [4].

This structure uses unique X-shaped inductance-capacitance (LC) impedance network that is connected between the DC link and the AC side. There are shoot-through states in Z-source inverter. These states boost voltage and LC impedance network prevent short circuit problems. Recently, new topologies of multilevel Z-source are introduced [7], [13]-[5]-[6].

These structures are used in clean energy harnessing such as photovoltaic (PV) arrays, fuel cells, etc that have low DC voltage [6]. Some papers attempt to introduce special structures to reduce the number of elements of multilevel Z-source inverter.

In this paper, a five-level Z-source Neutral Point Clamped inverter is used to introduce advantages and disadvantages of Space vector pulse width modulation.

1.1. Block Diagram of Proposed Work

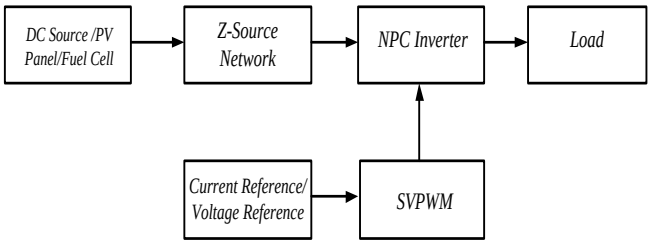


Figure 1. Block Diagram

The DC source may be any renewable DC source like solar photovoltaic or fuel cells. The Z source network exhibits both

voltage buck and voltage boost capability. The inverter that considered here is Neutral Point Clamped Inverter (NPCI) also known as Diode Clamped Multilevel Inverter (DCMLI) for three level output voltage. The modulation technique adopted is Space Vector Pulse Width Modulation (SVPWM).

2. MULTILEVEL INVERTER

Multilevel inverter obtain a desired output voltage from several level of input DC voltage Sources. With an increasing number of DC voltage Source ,the inverter voltage output will be nearly SINUSOIDAL .In recent years, the multilevel inverters are widely used in high power applications such as large induction motor drives, UPS systems, flexible AC transmission System (FACTS)

The term multilevel began with three level converter .However the elementary concept of multilevel converter to achieve higher power by using semiconductor switches with several lower voltage dc sources. Capacitors, batteries, and renewable energy voltage sources can be used as the multiple dc sources. The commutation of the power switches aggregate these multiple dc sources in order to achieve high voltage at output; however the rated voltage of the power semiconductor switches depends only upon the rating of the dc voltage sources to which they are connected.

The multilevel inverter has several outcomes over a conventional two-level converter that uses high switching frequency pulse width modulation (PWM).The attractive features of a multilevel converter can be briefly summarized as follows.

1. *Staircase Waveform Quality :*Multilevel converters not only can generate the output voltages with very low distortion ,but also can reduce the dv/dt stress therefore Electromagnetic compatibility EMC is reduced
2. *Common mode (CM) voltage :* Multilevel converter produces smaller CM voltage therefore the stress in the motor is reduced
3. *Input current :*Multilevel converter can draw input current with low distortion
4. *Switching Frequency:* MLI will operate in both fundamental and high switching frequency. Note that lower switching frequency usually means lower switching loss and higher efficiency

Classification of Multilevel Inverter Based On Source

Three different topologies have been projected for multilevel converters:

1. Diode clamped multilevel inverter (DCMLI)
2. Flying capacitor multilevel inverter (FCMLI)
3. Cascaded multilevel inverter (CMLI)

Several modulation and control strategies have been developed or being used for multilevel converters including the following

1. Multilevel sinusoidal pulse width modulation (MSPWM),
2. Multilevel selective harmonic elimination
3. Space-vector modulation (SVM).

2.1. Diode Clamped Multilevel Inverter

The widely used multilevel topology is the diode clamped inverter, in which the diode is used as the clamping device to clamp the dc bus voltage to achieve steps in the output voltage. Each of three phases of the six level inverter shares a common dc bus, which has been subdivide by five capacitors into six levels. The voltage across each capacitor is V_{dc} and the voltage stress across each switching device is limited to V_{dc} through the clamping diodes. State condition 1 means the switch is ON and 0 means the switch ids OFF. Each phase has fi9ve complementary switch pairs such that turning on one of the switches of the pair that the other complementary switch be turned OFF. In general the voltage across each capacitor for an N level diode clamped inverter at steady state is V_{dc}/n-1.

In general for a N level diode clamped inverter, for each leg 2(N-1) switching device,(N-1)*(N-2) clamping diodes and (N-1) dc link capacitors are required.

2.2. Flying capacitor multilevel inverter

The capacitor clamped inverter alternatively known as flying capacitor was proposed by Maynard and Foch .The flying capacitor involves series connection of capacitor clamped switching cells. The structure of this inverter is similar to that of the diode clamped inverter except that instead of using clamping diodes, the inverter uses capacitors in the place. The circuit topology has a ladder structure of dc side capacitor where the voltage on each capacitor differs from that of the next capacitor. One advantage of the flying capacitor based inverter is that it has redundancies can synthesize on output voltage .Unlike the diode clamped inverter, the flying capacitor inverter does not require all of the switches that are on be in a consecutive series

In addition to (m-1) dc link capacitors, the m-level flying capacitor multilevel inverter will require (m-1) x (m-2)/2 auxiliary capacitor per phase if the voltage rating of the capacitor is identical to that of the main switches.

2.3. Cascaded multilevel inverter

In single phase structure of an m-level inverter each separate dc source (SDCS) is connected to a single phase full bridge of

H-bridge, inverter .Each inverter level can generate three different voltage output $+V_{dc}$ 0 and $-V_{dc}$ by connecting the DC source to then AC output by different combination of the four switches S_1,S_2,S_3 and S_4.The AC output of each of the different full bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter output. The number of output phase voltage level m in a cascade inverter is defined by m = 2s+1, where is the4 number of separate DC sources. Multilevel cascaded inverter has been proposed for such application as static var generation, and interfaces with renewable energy sources and for battery based application. Cascaded inverter are ideal for connecting renewable energy sources with an AC grid, because of the need for separate DC sources, which is the case in application such as photovoltaic or fuel cells.

3. Z-SOURCE INVERTER

3.1. Introduction

There exist two traditional converters: voltage-source and current-source converters. The ac output voltage is limited below and cannot exceed. The dc-rail voltage has to be greater than the ac input voltage. Therefore, the V-source inverter is a buck inverter for dc-to-ac power conversion and the V-source converter is a boost rectifier for ac-to-dc power conversion An output LC filter is needed for providing a sinusoidal voltage compared with the current-source inverter, which causes additional power loss and control complexity. The dc current source can be a relatively large dc inductor fed by a voltage source such as a battery, fuel-cell stack, diode rectifier. To overcome the problems of the traditional V-source and I-source inverter a new concept was developed in year 2002 by Dr. F.Z. Peng. This involves combination of VSI and CSI to form a cross coupled network of two inductors and two capacitors, known as Impedance Network (Z-source network)

A Z-source inverter is a type of power inverter, a circuit that converts direct current to alternating current. It functions as a buck-boost inverter without making use of DC-DC Converter Bridge due to its unique circuit topology.

3.2. Working Principles of Z-Type Inverter

The figure presents a scheme of basic 3-phase Z-inverter. In distinction from VSI and CSI inverters, on DC side of Z-inverter occurs a D diode and a Z-source of "X" shape, composed of two capacitors *C1* and *C2* and two chokes *L1* and *L2*. The D diode prevents forbidden reversed current flow.

For this reason application of Z-inverter is possible only where there is no necessity for energy return to *UIN* source, further it is even forbidden in case of fuel cell or photo-voltaic cell. It should be marked that the same as D diode function can be server by other power electronics systems including ex. Diode rectifier or typical boost-converter".

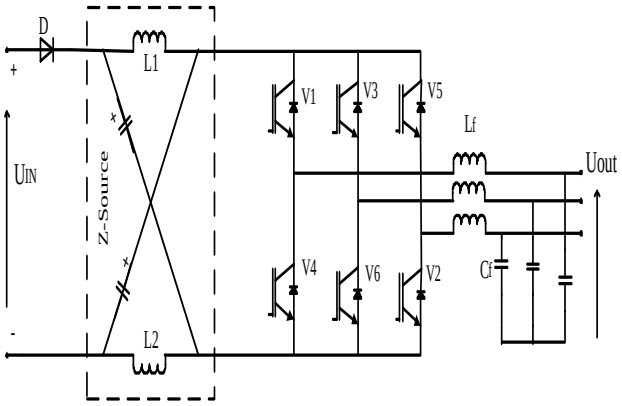
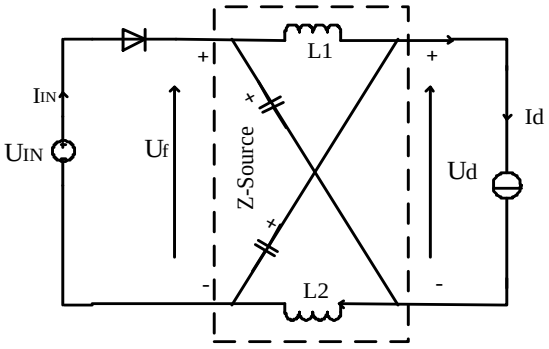


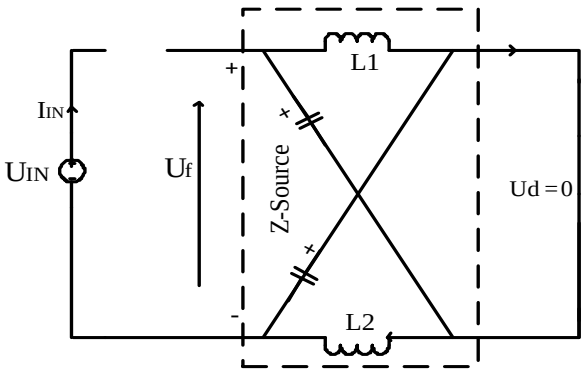
Fig 2. Basic Scheme of 3 –phase Z inverter

Source Z serves as power storage and guarantees double filtration grade at the input of the inverter, and therefore dumping current ripples and voltage pulsation in the DC circuit. Concluding, requirements for chokes and capacitors in Z-source are less restrictive than in VSI or CSI inverters. In a case where chokes *L1* and *L2* have very low inductance (≈0), Z-source is created only from parallel connected capacitors *C1* and *C2*. Then Z-inverter simply becomes VSI system and condensers in DC circuit are the only storage for energy and at the same point are a cell for filtration of voltage pulsation. Analogically when capacitors *C1* and *C2* are of low capacity (≈0), Z-source is diminished to two chokes *L1* and *L2* that are parallel connected, and Z-inverter system becomes CSI system. Chokes in DC circuit of CSI system and capacitors in DC circuit of VSI system must be of greater inductance and capacity (their dimensions) than in case of Z-inverter.

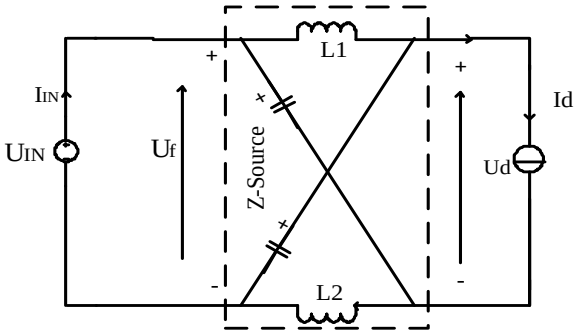
Typical 3-phase VSI system can assume eight allowed (permitted) states: six active states (while exchange of instantaneous power between the load and DC circuit) and two null states (when the load is shorted by lower or upper group of transistors). Whereas, 3-phase Z-inverter system can assume nine permitted states that is one more than in VSI system.



a) General configuration



b) In Shoot through state



c) In non-shoot through states

Figure 3. Equivalent schemes of Z-inverter

Additional ninth state is the third null state, occurring when the load is being shorted simultaneously by lower and upper group of transistors. This state, is defined as „ shoot-through "state and may be generated in seven different ways, however equivalent procedures: independently through every branch (3 procedures), simultaneously through two of the branches (3 procedures), simultaneously through all of the three branches (1 procedure). The main, unique characteristic of Z-inverter is that shoot-through state permits to rise output voltage, above the supply voltage U_{IN}

Figure 3 describes simple equivalent schemes of Z-inverter, examined from the clap site of DC, where a source u_d shapes inverter bridge V_1-V_6 . In the shoot-through states (Fig.4b) a D diode is polarized reversely and does not conduct the inverter bridge input voltage $u_d=0$, and energy stored in capacitors C_1 and C_2 is transferred to the chokes L_1 and L_2. In non-shoot-through" states, where every combination of the chokes V_1-V_6 that is allowed in VSI system is possible, the D diode conducts, and the voltage u_d increases stepwise from 0 to its maximum u_{d*}. Since Z-source is symmetric circuits, when C_1=C_2 and L_1=L_2 and low voltage pulsation U_{c1} and U_{c2} due to impulse period T,it can be recorded as

$$U_{C1} = U_{C2} = U_C \,,\; u_{L1} = u_{L2} = u_L \qquad (1)$$

where

U_C – mean value of voltage in capacitors,

u_L – instantaneous voltage in chokes.

Considering (1) and equivalent schemes of Z-inverter (Fig.4), voltage u_d is calculated on the basis of following dependences

(a) in shoot-through states (Fig.2b) in time T_Z

$$u_L = U_C \,,\; u_f = 2 \cdot U_C \,,\; u_d = 0 \qquad (2)$$

b) in "non-shoot-through" states (Fig.2c) in time T_N

$$u_L = U_{IN} - U_C \,,$$

$$u_f = U_{IN} \,,\; u_d = U_C - u_L = 2 \cdot U_C - U_{IN} \qquad (3)$$

where u_f – Z-source input voltage.

If taken into consideration, that in a time period $T = T_Z + T_N$, in steady state overage voltage in chokes $U_L=0$, then on the basis of (2) and (3) we obtain

$$U_L = \frac{T_Z . U_C + T_N . (U_{IN} - U_C)}{T} = 0 \qquad (4)$$

and

$$U_C = U_d = U_{IN} \cdot \frac{T_N}{T_N - T_Z} = U_{IN} \frac{1-D}{1-2.D}$$

where

$D=T_Z/T$-"shoot-through" coefficient, satisfying a condition $D<0.5$.

Similar procedure, on the basis (3) and (4) determines the value u_{d*} of voltage u_d in "non-shoot-through" states:

$$u_d^* = U_C - u_L = U_{IN} \frac{1}{1-2.D} \qquad (5)$$

where

$1/(1-2 \cdot D) = T/(T_N - T_Z) \geq 1$ - peak factor, determining the value u_{d*} voltage $U_{IN.}$

The value u_{d*} determines output voltage amplitude $u_{OUT(max)}$ of Z-inverter. When applying sinusoidal PWM algorithm the amplitude equals

$$U_{out(max)} = M . \frac{u_d^*}{2} = \frac{M}{1-2D} \cdot \frac{U_{IN}}{2} \qquad (6)$$

where M – modulation index, of maximum value limited by inequity $M \leq 1-D$, related to time T_Z of shoot through states. As it results from the equation (6), Z-inverter output voltage

amplitude $u_{OUT(max),}$ can be as well lower as higher than in typical VSI system with sinusoidal PWM,

$$u_{OUT\ (max)} = M \cdot U_{IN}/2.1$$

4. MODULATION TECHNIQUES

4.1. Sine-Triangle Pulse Width Modulation

The principle of the sinusoidal PWM scheme for the two-level inverter is illustrated in Fig-2, where V_{mA}, V_{mB}, and V_{mC} are the three-phase sinusoidal modulating waves and Vcr is the triangular carrier wave. The fundamental frequency component in the inverter output voltage can be controlled by amplitude modulation index,

$$ma = Vm / Vcr \quad (1)$$

Where Vm and Vcr are the peak values of the modulating and carrier waves, respectively. The amplitude modulation

Index ma is usually adjusted by varying Vm while keeping V_{cr} fixed. The frequency modulation index is defined by

$$mf = fm / fcr \quad (2)$$

Where, fm and fcr are the frequencies of the modulating and carrier waves, respectively. The gating signals for conventional two-level inverter using SPWM can be derived as follows. The operation of switches S1 to S6 is determined by comparing the modulating waves with the carrier wave. When $V_{mA} \geq V_{cr,}$ the upper switch S1 in inverter leg A is turned on. The lower switch S4 operates in a complementary manner and thus is switched off. The resultant inverter terminal voltage VAN, which is the voltage at the phase A terminal with respect to the negative DC-link bus 'N', is equal to the DC voltage Vd. When $V_{mA} < V_{cr,}$ S4 is on and S1 is off, leading to VAN = 0. Since the waveform of VAN has only two levels, Vd and 0, the inverter is known as a two level inverter.

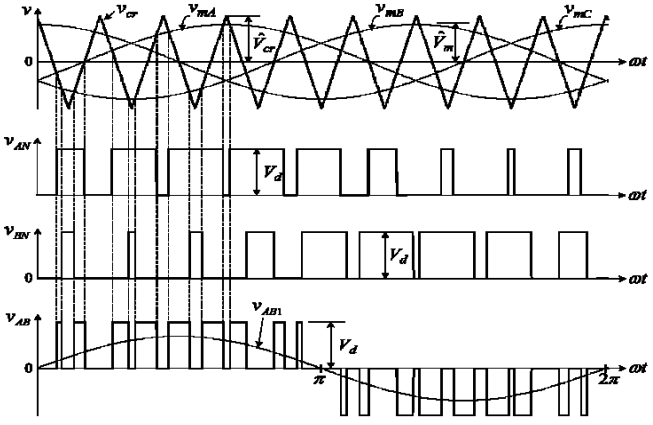


Fig 4. Sinusoidal Pulse Width Modulation

4.2. Space Vector Modulation

4.2.1. Introduction

Space vector modulation (SVM) is an algorithm for the control of pulse width modulation (PWM).[1] It is used for the creation of alternating current (AC) waveforms; most commonly to drive 3 phase AC powered motors at varying speeds from DC using multiple class-D amplifiers. There are various variations of SVM that result in different quality and computational requirements. One active area of development is in the reduction of total harmonic distortion (THD) created by the rapid switching inherent to these algorithms.

4.2.2. Space Vectors

The technique of the space vector modulation involves the concept of space vector. In any three phase machine, the stator coils are distributed in space in a symmetrical manner i.e. each coil is placed at 120 degree with respect to each other. In this method the five phase quantities can be transformed to their equivalent 2-phase quantity either in synchronously rotating frame or stationary reference frame.

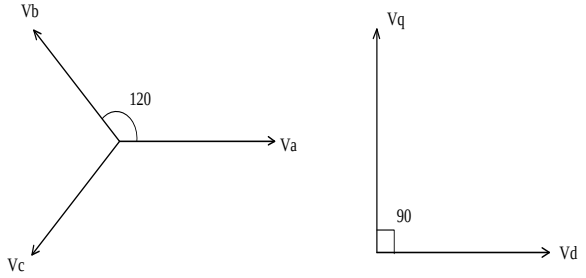


Figure 5. Three Phase Quantities Transformed into Two Phase

From this 2-phase component the reference vector magnitude can be found and used for modulating the inverter output. Let the three phase sinusoidal voltage component be,

$$V_a = V_m \sin \omega t$$

$$V_b = V_m \sin (\omega t - 120)$$

$$V_c = V_m \sin (\omega t - 240)$$

Equating the three phase machine quantities, we get

$$V_a + V_b + V_c = 0 \quad (1)$$

$$Vd = -3/2(Vb) + 3/2(Vc) = 3/2Vm\cos\omega t \quad (2)$$

$$Vq = Va - Vb/2 - Vc/2 = 3/2Vm\sin\omega t \quad (3)$$

Rotating vector,

$$Vref=Vd=Vq=3/2e^{(j\omega t)} \quad (4)$$

From equation (4) it can be seen that space vector moves with constant angular velocity and constant amplitude. In case of non-sinusoidal quantities, the space vectors will not necessarily move with constant amplitude or constant angular velocity. The output of the inverters which are usually used in various applications are not perfectly sinusoidal. It contains appreciable amount of harmonics. So, the space vector of the stator voltages in these cases if of amplitude Vdc moving in steps and not with a constant angular velocity. In space vector modulation, a reference vector of the stator voltages is generated, which is made to move in the d-q plane in small steps so that it appears to move smoothly, as in the case with sinusoidal supply. The space vector modulation is based on the space vector representation of the voltages in d-q plane. After the transformation to the two phase quantities, the power as well as the impedance remains unchanged. In space vector modulation we try to generate a voltage reference vector at a point of time and the voltage reference vector Vref is sampled which approximately by a time sequence of five well defined switching state vector nearest to the reference vector. This is done by sampling the switching state vectors in such a way that the total volt seconds generated by these vectors over an interval Ts equals the volt seconds generated by the reference vector Ts.

4.2.3. Design Procedure

Step I

To assume the Peak voltage value (Vm)

Time period (t)

Delta ($\pi/2$)

Step II To Calculate the Vref Values

$Va\_ref = Vm \sin(\omega t + \pi/2)$

$Vb\_ref = Vm \sin(\omega t - 2\pi/3 + \pi/2)$

$Vc\_ref = Vm \sin(\omega t + 2\pi/3 + \pi/2)$

Step III

(i) To transfer the abc Parameters into dq Parameters

(ii) To find the magnitude and theta values from dq Parameters

Va Vb Vc ⟶ Vq & Vd ⟶ Magnitude & theta

Step IV Identification of Sectors from theta values

Theta ⟶ Sector Identification and ensure each sector having angle of 60°each (theta1)

$\beta = \text{int}[\theta/60] + 1$

$\gamma = \text{rem}[\theta/60] = \theta_1$

Step V To find the Magnitude of Vαref and Vβref & Theta 1

$V\alpha = Vm \cos[\theta 1 * \pi/180]$

$V\beta = Vm \sin[\theta 1 * \pi/180]$

Step VI Identification of Sectors by using K_1 and K_2 values

$K_1 = \text{int}\left[V_\alpha + V_\beta/\sqrt{3}\right]$

$K_2 = \text{int}\left[2V_\beta/\sqrt{3}\right]$ K_1 & K_2 are integers

Step VII

To find $V_{\alpha i}$ and $V_{\beta i}$

$V_{\alpha i} = V\alpha - K_1 + 0.5K_2$

$V_{\beta i} = V\beta - K_2 h = V\beta - \sqrt{3}K_2/2$

$(h = \sqrt{3}/2)$

Step VIII

To find the location of Reference vector P

Case I

If $\sqrt{3}\, V_{\alpha i} \geq V_{\beta i}$ or $\sqrt{3}\, V_{\alpha i} \leq V_{\beta i}$

1. True means P is at Δ1
2. False means P is at Δ2

Step IX

To find out the type of triangle (Type I or Type 2)

(i) P at Δ2 common for type 2 triangle

$V_{\alpha 0}^{S} = 0.5 - V_{\alpha i}$

$V_{\beta 0}^{S} = \sqrt{3}/2 - V_{\beta i}$

(ii) P at Δ1 common for type 1 triangle

$V_{\alpha 0}^{S} = V_{\alpha i}$

$V_{\beta 0}^{S} = V_{\beta i}$

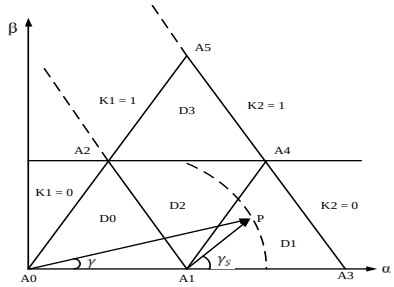


Figure 6 Determination of Triangle

Step X Triangle number calculation

For type I triangle

$$\Delta j = K_1^2 + 2K_2$$

For type II triangle

$$\Delta j = K_1^2 + 2K_2 + 1$$

Step XI

Determination of ON time by two level SVPWM unit

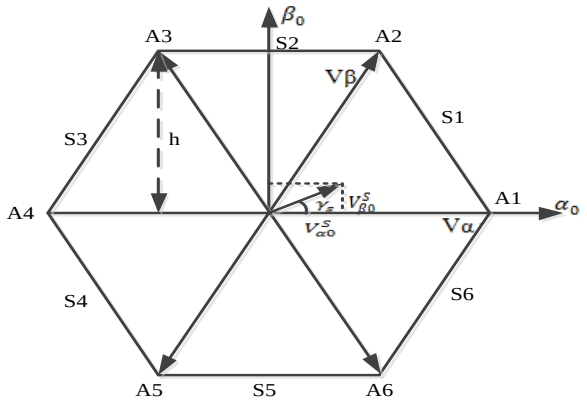


Fig 7 Space Vector Representation of Two Level Inverter

$V\alpha = (1,0)$

$V\beta = (0.5, h)$

$$V^s = (V_{\alpha 0}^S \; V_{\beta 0}^S)$$

Space vector diagram for two level inverter by using this diagram the volt second balance is given by

$$V^s T_S = V_a t_a + V_b t_b$$

Time balance is given by

$$T_S = t_a + t_b + t_0$$

In $\alpha_0 - \beta_0$ axis

$$V_{\alpha 0}^S T_S = 1.\, t_a + 0.5\, t_b$$

$$= t_a + 0.5\, t_b$$

$$V_{\beta 0}^S T_S = \text{h}.t_b + 0.\, t_a$$

$$= \text{h}.t_b$$

because $V\alpha = (1,0)$

$V\beta = (0.5, h)$

$$V^s = (V_{\alpha 0}^S \; V_{\beta 0}^S)$$

Calculation of ON time

$$V_{\alpha 0}^S T_S = t_a + 0.5\, t_b$$

$$V_{\beta 0}^S T_S = \text{h}.t_b$$

$$t_b = \frac{V_{\beta 0}^S T_S}{h}$$

Therefore

$$t_a = V_{\alpha 0}^S T_S - 0.5 \frac{V_{\beta 0}^S T_S}{h}$$

$$= T_s \left\{ V_{\alpha 0}^S - \frac{V_{\beta 0}^S T_S}{2h} \right\}$$

$$t_0 = T_s - t_a - t_b$$

Step XII

Generation of gating signals

4.2.4. Circuit Diagram of Proposed System

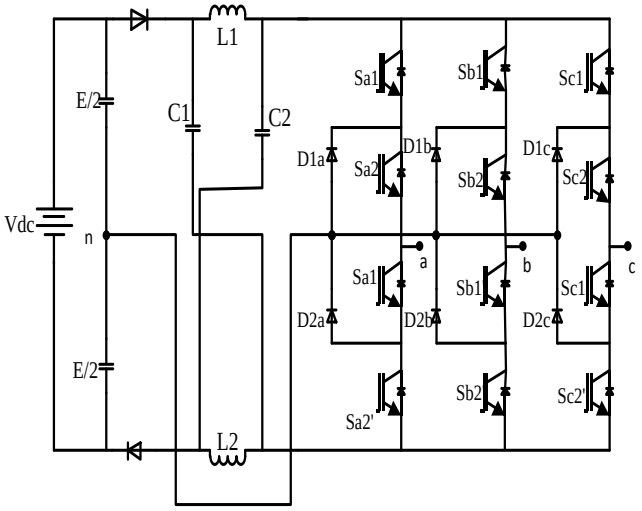


Fig 8 Proposed Circuit Diagram of ZNPC

The circuit diagram of proposed system shows five level Z-source NPC inverter where the only difference compared with the traditional inverters is the inserted Z-source network and a passive diode D between dc supply and inverter circuitry. The two-port network is built using a split inductor and two shunt capacitors, whose X-shape structure allows switches from any phase-leg to turn ON simultaneously with the input diode D naturally reverse-biased to create a shoot through state without

damaging the semiconductor device due to natural property of current production by inductors.

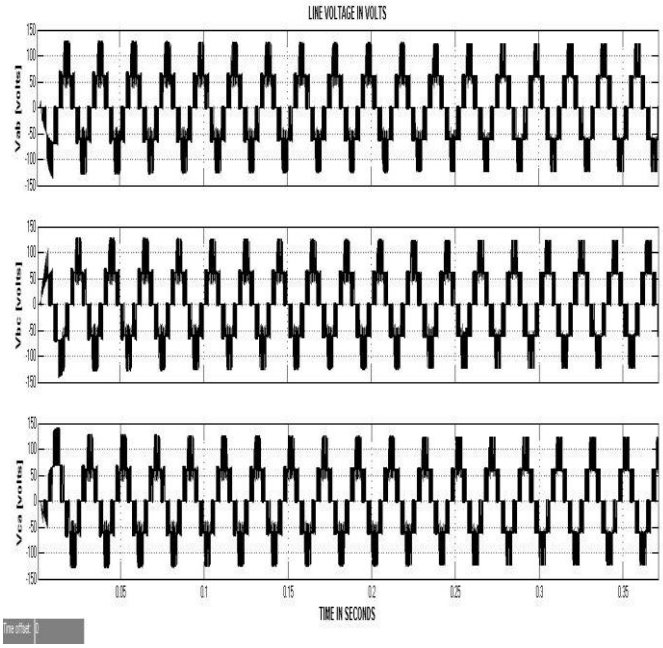
5. RESULTS AND DISCUSSIONS

Here the Z source Neutral Point Clamped Inverter using Space Vector Pulse Width Modulation Technique with PV panel as source is implemented. The performance parameters like Phase voltage, Line voltage Load current and THD are analyzed using MATLAB Simulink and the result are given below:

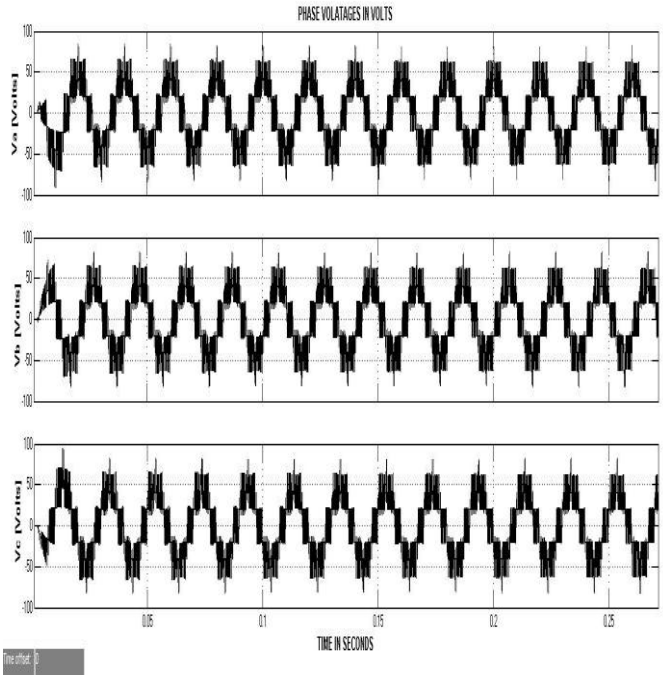
(a)

(b)

Figure 9. Simulated (a) Line Current and (b) Phase Current Waveform

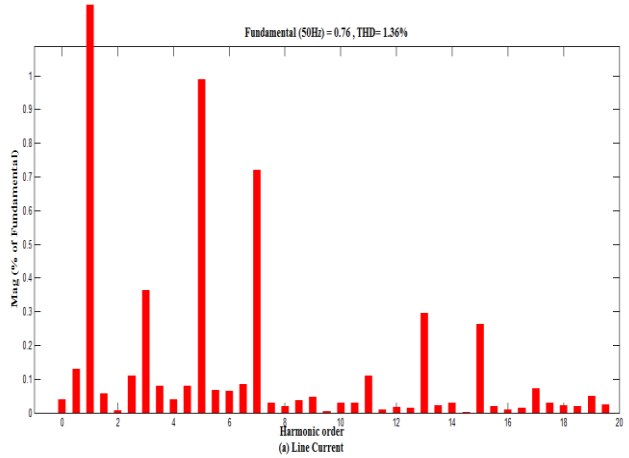


(a)

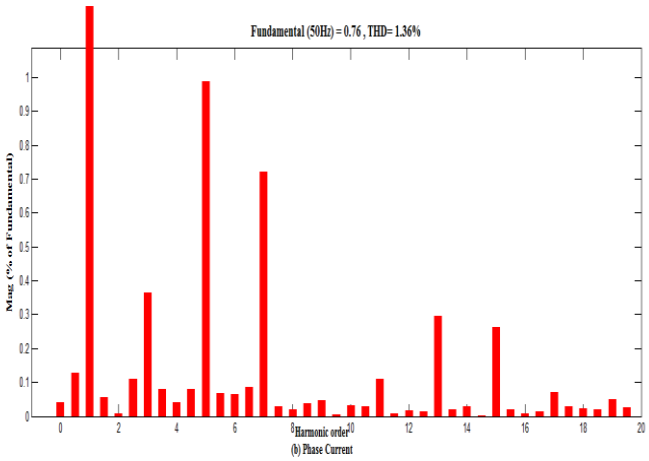


(b)

Figure 10 Simulated (a) Line Voltage and (b) Phase Voltage Waveform

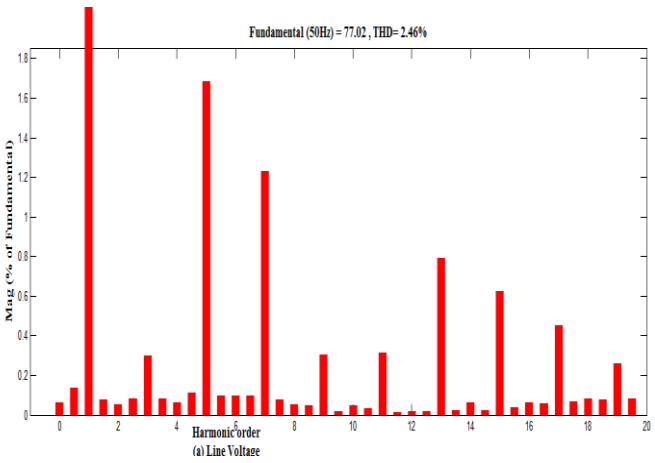


(a)

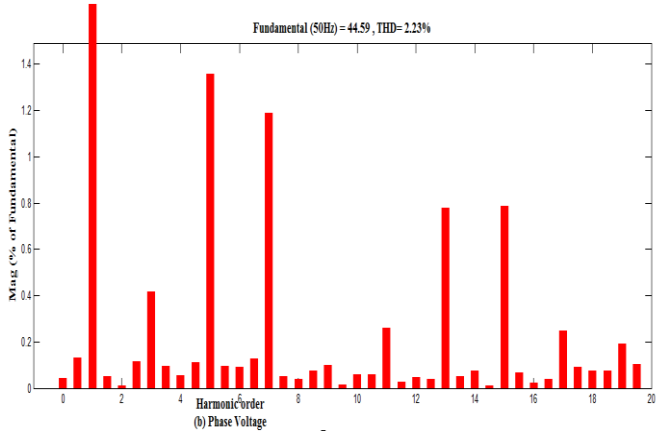


(b)

Figure 11 FFT Plot for output (a)Phase Current (b) Line Current of Five level ZNPC (PV Source) inverter using SVPWM technique



(a)



(b)

Figure 12 FFT Plot for output (a) Line Voltage and (b)Phase Voltage of Five level ZNPC (PV Source) inverter using SVPWM technique

5.1. Comparison of SPWM and SVPWM techniques by analyzing various parameters

S.No	***Performance Analysis Parameters***	***Sinusoidal PWM Technique***	***SV PWM Technique (DC Source)***	***SVPWM with PV Panel as Source***
1	Phase Voltage Magnitude	62	72	81
2	Phase Current Magnitude	0.9	0.75	0.9
3	Line Voltage	107	120	140
4	Line Current	0.9	0.75	0.9
5	Phase voltage THD	9.45%	6.81%	2.23%
6	Phase Current THD	3.85%	3.36%	1.36%
7	Line Voltage THD	9.41%	6.72%	2.46%
8	Line Current THD	3.85%	3.36%	1.36%

Table 1.Comparison of SPWM and SVPWM Techniques

S.No	***Switching frequency (f =1/T)***	***Line Voltage THD***	***Line Current THD***	***Phase Voltage THD***	***Phase Current THD***
1	*1/3000 = 3.333 KHz*	*2.46%*	*1.36%*	*2.23%*	*1.36%*
2	1/3500 = 2.857 KHz	4.83 %	3.02%	7.39%	3.02%
3	1/4000 = 2.5 KHz	9.35%	5.89%	10.90 %	5.89%
4	1/4500 = 2.222 KHz	6.67%	4.26%	6.16%	4.26%
5	1/5000 = 2 KHz	6.01%	3.92%	6.87%	3.92%

Table 2 THD Analysis of Various Switching frequencies

From the above analysis we conclude that Space Vector PWM technique is more superior to the Sinusoidal PWM technique for multilevel inverter in various industrial application.

6. CONCLUSION

This paper presents the design of a Z-source NPC inverter that can perform buck-boost dc-ac energy inversion. Under special operations with respect to the partial dc-link shoot-through, which profitably appear in the operation of Z-source NPC inverter, the Z-source network shows much different operational principles and boost characteristics. Modulation wise, the proposed inverter can be controlled using Space Vector Modulation techniques with a slight modification of three-phase references. The theoretical findings, together with the practicality of the inverter, have been analysed using PSIM and MATLAB/Simulink model under both normal and voltage boost conditions.

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